RECEIVED
CENTRAL FAX CENTER

JUN 20 2007

Turin 1999-0078con

REMARKS

Claim 23 was objected to because of a typographical error. The error is corrected herein.

Claim 25 was rejected on the ground of nonstatutory obvious-type double patenting in view of claim 2 of US Patent 6,700,937. The rejection is overcome with a Statutory Disclaimer that is filed herewith.

Claim 25 was rejected under 35 USC 112, first paragraph. The Examiner asserts that the claimed subject matter "memory containing an instruction module that performs process steps" lack support in the original disclosure.

Applicant respectfully traverses. From the fact that claim 25 was rejected on the ground of nonstatutory obvious-type double patenting in view of method claim 2 of the parent application, and from the fact that the Examiner's comment focuses on the fact that the claim focuses on memory, applicants surmise that the memory where the instruction module reside is the true issue.

Reviewing the teachings in this case, use of a receiver 104 is taught at page 2, line 19, of the application. Also at page 2 of the application (line 25 et seq.) it is taught that MAP decoding is a technique that decodes a received sequence. Hence, the MAP decoding is performed in the receiver. Much of the following text is devoted to the MAP decoding per se, until at page 11 a specific embodiment of a receiver is depicted. It is depicted to contain a controller, a forward processor, a backward processor, a maximal length processor, and a memory 204 (in addition to an input/output device). Illustratively, controller 202 is a digital signal processor (DSP), which possesses no memory to speak of, and the other processors are ASICs PLAs PLDs, which also possess no memory to speak of. A DSP is a device that is constructed to perform various generic functions. A specific method is caused to be executed by DSP 202 only with the aid of a stored program that dictates execution of each of the method steps; in other words, a module of instructions. The same is true about the other processors, although in a different sense. That is, a PLA, for example, is designed to implement a certain specific functionality, but unless that functionality is nothing but a combinatorial logic block, it must include memory. A PLD (Programmable Logic Device) is a device that inherently contains programming memory, and an ASIC also inherently contains memory elements.

Turin 1999-0078con

Thus, the method that is executed in the receiver that is described in the parent application is controlled by information that is maintained in a memory; either all in memory 204 of in a memory that is a combination of the memories within the processors together with memory 204.

The above notwithstanding, claim 25 is amended and, as amended, it is believed that it is even more clearly supported by the parent application.

Claim 23 was rejected under 35 USC 102 as being anticipated by Abbaszadeh, US Patent 6,563,887. Applicant respectfully traverses. The Examiner points to prior art that is discussed in the Abbaszadeh reference and ends with the statement that

> In view of that, the decoding output is maximized over probability distribution over the inner code alphabet conditioned on the received signal The algorithms are performed through iterates stage decoding; see column 3, lines 1-5.

The cited passage (extended to the beginning and end of sentence) teaches

> The resulting concatenated coding scheme is a power full code endowed with a structure that facilitates decoding, such as by using so-called stage decoding or iterative stage decoding.
>
> In order to function properly these decoding algorithms cannot limit themselves to simply passing the symbols decoded by an inner decoder to an outer decoder.

The term "iterative stage decoder" is not mentioned anywhere else in the reference, and it certainly is not explained in the cited passage. Hence, it is not known what is meant by it. Moreover, nowhere in the reference is there any teaching of

(a) a "probability distribution matrix,"

(b) a "probability distribution matrix $\mathbf{P}(X,Y)$," where X represents a sent information signal and Y represents the received information signal,

(c) an "auxiliary function that includes a product of elements $p_{ij}(X,Y)$ of a probability distribution matrix $\mathbf{P}(X,Y)$, or

(d) maximizing this auxiliary function -- iteratively or otherwise.

It is respectfully submitted, therefore, that claim 23 is not anticipated by the Abbaszadeh reference.

Claim 24 was objected to for being dependent on a rejected base claim, but it was indicated to be allowable is converted to independent form. This has been effected.

Turin 1999-0078con

In light of the above amendments and remarks, applicant respectfully submits that all of the Examiner's rejections and objections have been overcome. Reconsideration and allowance are respectfully solicited.

Respectfully,
William Turin

Dated: 6/20/07

By: Henry Brendzel

Henry T. Brendzel
Reg. No. 26,844
Phone (973) 467-2025
Fax (973) 467-6589
email brendzel@comcast.net